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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/621,364	07/18/2003	Toshihiro Yanagi	12480-000018US	4032

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EXAMINER	
SHERMAN, STEPHEN G	

ART UNIT	PAPER NUMBER
2674	

DATE MAILED: 09/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/621,364	YANAGI ET AL.	
	Examiner	Art Unit	
	Stephen G. Sherman	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 July 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 14404, 7-18-03
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figures 3a and10-16 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

2. The drawings are objected to because Figure 7 is not referenced in the specification. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the

drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. The abstract of the disclosure is objected to because of undue length. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims ~~1-6~~ 1,2,4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over APA (Figure 12 and Page 4 line 10 to Page 5 line 16 of the specification) in view of Chee (US 6,088,806) and further in view of Ranganathan (US 5,615,376).

Regarding claim 1, APA discloses a display device which selects each line of a screen having pixels aligned in a matrix manner and provided in a display section by applying a scanning signal to a scanning signal line of a pixel of each line so as to scan the screen, and supplies a data signal from a data signal line to a pixel of a selected line so as to carry out display (Page 4, line 25 to Page 5, line 5) comprising: a driving control circuit (Figure 12, item 109) which stops driving of driving circuits provided for driving the display section, the driving control circuit stopping driving of the driving circuits in an inaction period where all scanning lines become non-scanning state, the inaction period being provided between scanning periods for scanning the screen (Page 4, lines 10-19 and Page 5, lines 6-16). APA fails to teach of a clock signal generation circuit for generating a clock signal which is used for taking the data signal into the data signal line, the driving control circuit stopping driving of the clock signal generation circuit. Chee discloses of a clock signal generation circuit (Figure 4, item 44) for generating a clock signal which is used for taking the data signal into the data signal line, the driving control circuit stopping driving of the clock signal generation circuit (Column 4, lines 64-67 and Column 5 lines 1-5. The examiner interprets the power-down circuitry to be the driving control circuit.). Therefore it would have been obvious to "one of ordinary skill" in the art to combine the teachings of APA and Chee in order to create a display device capable of realizing a reduction of power consumption. APA and Chee fail to teach of stopping driving of the clock signal of the clock signals in the inaction period (Column 3, lines 2-15 and Column 4, lines 66-67. The examiner interprets that pausing of the clock stated in column 3 would consist of stopping driving of the clock since in column 4 it is

stated that clocking of circuitry is disabled.). Therefore it would have been obvious to "one of ordinary skill" in the art to combine the teachings of APA, Chee and Ranganathan in order to create a display device capable of realizing a reduction of power consumption during periods in which the circuits are not being used during a time in which the display device is active but are enabled only when it is necessary to refresh the display screen.

Regarding claim 2, APA, Chee and Ranganathan disclose the display device as set forth in claim 1. Chee also discloses the display device further comprising: an output timing clock generation circuit for generating an output timing signal of a driving signal to the display section from the driving circuits, wherein: the clock signal generation circuit generates the clock signal based on the output timing clock generated by the output timing clock generation circuit, and the driving control circuit stops driving of the output timing clock generation circuit in the inaction period (Column 4, lines 64-67 and Column 5, lines 1-5. The examiner interprets that since the power-down circuitry is capable of sending an enable/disable signal to the clock generator and that the clock generation circuit is then able either to send or not to send a clocking signal to the circuitry of the monitor, that it would contain an output timing clock generation circuit to create the timing that the clock generation circuit would then send to the monitor.) . Therefore it would have been obvious to "one of ordinary skill" in the art to combine the teachings of APA, Chee and Ranganathan in order to create a display device capable of realizing a reduction of power consumption during periods in which the circuits are not

being used and when the circuits are being used, to output a clock signal containing the correct output timing for the driving circuits.

Regarding claim 4, APA, Chee and Ranganathan disclose the display device as set forth in claim 1. APA also discloses the display device wherein: the clock signal generation circuit is a clock signal oscillation circuit for oscillating a clock signal (Figure 12, item 106).

Regarding claim 5, APA, Chee and Ranganathan disclose the display device as set forth in claim 1. APA also teaches of liquid crystal display elements being used as the pixels ().

Regarding claim 6, APA discloses a driving method for a display device which selects each line of a screen having pixels aligned in a matrix manner by applying a scanning signal to a scanning signal line of a pixel of each line so as to scan the screen, and supplies a data signal from a data signal line to a pixel of a selected line so as to carry out display (Page 4, line 25 to Page 5, line 5), wherein: an inaction period is provided between the scanning periods for scanning the screen (Page 4, lines 10-19). APA fails to teach a driving method for a display device wherein driving of a clock signal generation circuit for generating a clock signal which is used for taking the data signal into the data signal line is stopped. Chee discloses a driving method for a display device wherein driving of a clock signal generation circuit (Figure 4, item 44) for generating a clock signal which is used for taking the data signal into the data signal line is stopped (Column 4, lines 64-67 and Column 5 lines 1-5. The examiner interprets the power-down circuitry to be the driving control circuit.). Therefore it would have been

obvious to "one of ordinary skill" in the art to combine the teachings of APA and Chee in order to create a display device capable of realizing a reduction of power consumption. APA and Chee fail to teach a driving method for a display device wherein the driving of a clock signal is stopped during an inaction period. Ranganathan discloses a driving method for a display device wherein the driving of a clock signal is stopped during an inaction period (Column 3, lines 2-15 and Column 4, lines 66-67. The examiner interprets that pausing of the clock stated in column 3 would consist of stopping driving of the clock since in column 4 it is stated that clocking of circuitry is disabled.). Therefore it would have been obvious to "one of ordinary skill" in the art to combine the teachings of APA, Chee and Ranganathan in order to create a display device capable of realizing a reduction of power consumption during periods in which the circuits are not being used during a time in which the display device is active but are enabled only when it is necessary to refresh the display screen.

6. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over APA (Figure 12 and Page 4 line 10 to Page 5 line 16 of the specification), Chee (US 6,088,806) and Ranganathan (US 5,615,376) and further in view of Tsuda et al. (US 2002/0180673). APA, Chee and Ranganathan disclose the display device as set forth in claim 2. APA, Chee and Ranganathan fail to teach of the display device further comprising: a start timing clock generation circuit for generating a start timing clock which is used as a scanning start timing signal of the driving circuits, wherein: the output timing clock generation circuit generates the output timing clock based on the start

timing clock generated in the start timing clock generation circuit, and the driving control circuit stops driving of the start timing clock generation circuit in the inaction period. Tsuda et al. disclose a display device comprising: a start timing clock generation circuit for generating a start timing clock which is used as a scanning start timing signal of the driving circuits (Paragraph [0107]. The examiner interprets that since the gate driver starts scanning in response to a gate start pulse signal receiver from the control IC, that the control IC contains a start timing generation circuit to create the signal. The examiner also interprets that when combined with the circuits of Chee that this gate start pulse signal, start timing signal, would cause the clock enabling signal to be sent to the output timing clock and that during the inaction period the power-down circuitry would also stop the driving of the start timing clock generation circuit, the control IC.). Therefore it would have been obvious to "one of ordinary skill" in the art to combine the teachings of APA, Chee, and Ranganathan in order to create a display device capable of realizing a reduction of power consumption during periods in which the circuits are not being used and when the circuits are being used, to output a clock signal in response to a start signal, containing the correct output timing for the driving circuits.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen G. Sherman whose telephone number is (571) 272-2941. The examiner can normally be reached on M-F, 8:00 a.m. - 4:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Patrick Edouard can be reached on (571) 272-7603. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SS

16 September 2005

REGINA LIANG
PRIMARY EXAMINER